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VLSI DESIGN AND IMPLEMENTATION OF LOW POWER, HIGH SPEED UNIT OF DECIMATOR USING MULTIRATE DSP

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Abstract

A Paper Presents Multirate DSP and its technique of the system which includes sampling rate conversion. This technique is necessary for systems with different input and output sampling rates, as the proposed multirate device is Decimator; FIR filter with downsampler is required, Simulation done on Active HDL and ALTERA QUARTUS–II platform. The circuit obtained is verified and implemented successfully. Then it is synthesized using 45 nm library in synopsis tool with constraint of low power and area with high speed. The circuit uses optimization to obtain a very low power. Reduction of power consumption is important for VLSI system and also it becomes one of the most critical design parameter. There are many reasons to change the sample rate of a sampled data signal. Here, author discuss the basic operation of a multirate system i.e. decimation. Also the use of multirate filters at the interfaces of continuous & sampled data which results in a cost reduction components as well as improvement of signal quality.

Keywords: VLSI-Very large scale integrated circuit, PCS -Personal communication services-, Active HDL-Hardware description language, RTL-Register transfer logic, DSP-Digital signal processing, VHDL-Very high speed hardware description language